R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus generally comprising a low speed tester and a host emulator. The host emulator may have (i) a first interface coupled to the low speed tester to receive a test vector at a first speed, (ii) a second interface configured to (a) transmit the test vector to a device at a second speed faster than the first speed and (b) receive a response from the device and (iii) a third interface to the low speed tester to transfer a signal based upon the response, wherein the apparatus is configured to allow the low speed tester to perform high speed tests of the device at the second speed.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 15-20, page 8 lines 7-13, page 10 lines 20-21 and in FIGS. 1 and 3, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 8-11 and 13-20 under 35 U.S.C. §102(a) as being anticipated by "SBAE-10 Bus Analyzer-Exerciser User's Manual" and "Analyzer/Exercise/Tester"

specification sheet, both by Catalyst Enterprises, Inc. (hereafter Catalyst) has been obviated by appropriate amendment and should be withdrawn.

Catalyst discloses a bus analyzer/exerciser/tester system. Catalyst does not appear to disclose or suggest every element as presently arranged in the claims. As such the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 1 provides a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector and (iii) a third interface to the low speed tester to transfer a signal based upon a response from a device. In contrast, Catalyst appears to disclose only a single interface between the SBAE-10 and a Windows Based System (i.e., a personal computer). Therefore, Catalyst does not appear to disclose or suggest a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector and (iii) a third interface to the low speed tester to transfer a signal based upon a response from a device as presently claimed.

Claim 1 further provides the host emulator having (i) a first interface coupled to the low speed tester to receive the test vector at a first speed and (ii) a second interface configured to (a) transmit the test vector to the device at a second speed faster than the first speed. In contrast, Catalyst appears to be silent

that any test vectors transferred from the Windows Based System to the SBAE-10 are slower than transmissions of the test vectors from the SBAE-10 to a USB Device Exercised. Furthermore, since another USB bus is a possible interface between the Windows Base System and the SBAE-10, Figure 3 of Catalyst appears to suggest that the test vectors provided by the Windows Based System are transferred to the SBAE-10 at the same speed as the SBAE-10 transfers the test vectors to the USB Device Exercised. Therefore, Catalyst does not appear to disclose or suggest a host emulator having a first interface coupled to a low speed tester to receive a test vector at a first speed and a second interface configured to transmit the test vector to a device at a second speed faster than the first speed as presently claimed. Claims 15 and 16 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 8 provides that the apparatus is configured to test a reception and transmission operation of the device. Page 3, lines 1-3 of the Office Action cite Catalyst (User's Manual) pages 39-40 as disclosing test packets for a transmission/reception loop. The cited text from Catalyst for "loop" reads:

> You may set up your exerciser program to operate in a loop by double clicking the left loop box for the line where the loop is to start and the right loop box for the line [w]here the loop is to end.

Nothing in the above text appears to disclose or suggest a transmission/reception loop. Instead, the above text appears to

indicate that an exerciser program may contain loops between two user selected lines of the program. Looping between lines of a program does not disclose a transmission/reception loop between the SBAE-10 and the USB Device Exercised. Therefore, the Office Action has failed to establish *prima facie* anticipation for lack of evidence that Catalyst discloses or suggests an apparatus configured to test a reception and transmission operation of the device as presently claimed. As such, claim 8 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 10 provides that the device is configured to receive and verify one or more test packets. In contrast, Catalyst appears to be silent regarding the USB Device Exercised verifying any test packets. Therefore, Catalyst does not appear to disclose or suggest a device configured to receive and verify one or more test packets as presently claimed. Furthermore, the Office Action does not provide any evidence that Catalyst anticipates claim 10. The Examiner is respectfully requested to either (i) withdraw the rejection or (ii) provide a clear explanation how Catalyst discloses the elements of claim 10.

Claim 11 provides that the device is configured to transmit one or more test packets. In contrast, Catalyst appears to be silent regarding the USB Device Exercised transmitting test packets. Therefore, Catalyst does not appear to disclose or suggest a device configured to transmit one or more test packets as

presently claimed. Furthermore, the Office Action does not provide any evidence that Catalyst anticipates claim 11. The Examiner is respectfully requested to either (i) withdraw the rejection or (ii) provide a clear explanation how Catalyst discloses the elements of claim 11.

Claim 13 provides that the low speed tester is configured to generate a pass/fail signal. Despite the assertion on page 2, last three lines of the Office Action, Catalyst appears to be silent regarding generation of a pass/fail signal. To the contrary, Catalyst appears to provide test data to a user leaving the user to decide pass or fail. Therefore, Catalyst does not appear to disclose or suggest a low speed tester configured to generate a pass/fail signal as presently claimed. As such, claim 13 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 14 provides that the apparatus is configured to perform at least one test of a plurality of test modes wherein the plurality of test modes comprise USB 2.0 defined test modes for use in a production test environment. In contrast, page 1 of Catalyst (specification sheet) states that the SBAE-10 is designed to be upgradable to USB 2. Therefore, the March 2000 documents from Catalyst do not disclose any details of the USB 2.0 specification that was not published until April 2000. In particular, Catalyst appears to be silent regarding USB 2.0 defined test modes for use

in a production test environment as presently claimed. Claim 20 provides language similar to claim 14. As such, claims 14 and 20 are fully patentable over the cited references and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 4-7 and 12 under 35 U.S.C. §103(a) as being unpatentable over Catalyst in view of Agrawal et al. '567 (hereafter Agrawal) has been obviated by appropriate amendment and should be withdrawn.

Catalyst teaches a bus analyzer/exerciser/tester system. Agrawal teaches delay testing of high-performance digital components by a slow-speed tester (Title). Catalyst and Agrawal, alone or in combination, do not appear to teach or suggest the elements as presently claimed. Furthermore, no clear and particular motivation has been provided to combine Catalyst and Agrawal. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 4 provides a test vector generator. Despite the assertion on page 3, last two lines of the Office Action, Agrawal appears to be silent regarding a test vector generator. The text of Agrawal cited by the Office Action reads:

> In step 520, the ATE 15 applies a suitable test stimulus to the master input 21 over the input line 12. As described in Agrawal & Seth, supra, a test stimulus may comprise one or more functional inputs or test vectors which are applied to

> a primary input of a circuit for detecting stuck-at faults and testing the propagation delay in a combinational logic block in the circuit.

Nothing in the above text, or the rest of Agrawal, states that the ATE 15 generates the test vectors. Therefore, Catalyst and Agrawal, alone or in combination, do not appear to teach or suggest a test vector generator as presently claimed. As such, claim 4 is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher (MPEP §2142). In particular, page 4, lines 9-10 of the Office Action state that motivation exists in Agrawal "for performing the automatic adjusting for high speed testing of Catalyst (column 3, lines 50-64)." The cited text of Agrawal reads:

> An automatic test equipment (ATE) apparatus tests the high speed operation of a circuit by applying test vectors and

> clocking signals to the primary inputs of a circuit in accordance with well known test methodologies, such as the techniques described in V. D. Agrawal and S. C. Seth, Test Generation for VLSI Chips, IEEE Computer Society Press, Los Alamitos, Calif. (1988), pp 327-331, which is incorporated by reference herein. The ATE then compares the signal response that appears at a primary output of the circuit to an expected correct response which is simulated based on the design of the circuit under test. Any mismatch between the monitored and expected response indicates the presence of one or more faults, such as, for example, a single stuck-at fault or a path delay fault, in the combinational logic or flip-flop elements of the circuit.

Nothing in the above text states that the test equipment performs "automatic adjusting for high speed testing" as asserted in the Office Action. The motivation appears to be merely a conclusory statement lacking support in the references. Therefore, the Office Action has failed to establish *prima facie* obviousness for lack of clear and particular evidence to combine the references. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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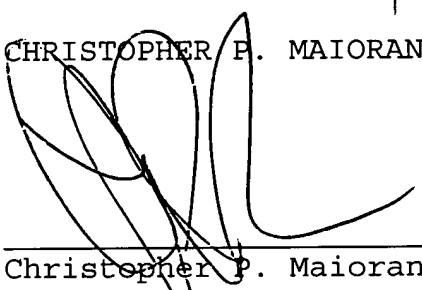

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